

Review of Five-Level Front-End Converters for Renewable Energy Applications

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Abstract

With the objective of minimizing environment and energy issues, distributed renewable energy sources have reached remarkable advancements along the last decades, with special emphasis on wind and solar photovoltaic installations, which are deemed as the future of power generation in modern power systems. The integration of renewable energy sources into the power system requires the use of advanced power electronics converters, representing a challenge within the paradigm of smart grids, e.g., to improve efficiency, to obtain high power density, to guarantee fault-tolerance, to reduce the control complexity and to mitigate power quality problems. This paper presents a specific review about front-end converters for renewable energy applications (more specifically the power inverter that interfaces the renewable energy source with the power grid). It is important to note that the objective of this paper is not to cover all types of front-end converters; the focus is only on single-phase multilevel structures limited to five voltage levels, based on a voltage-source arrangement and allowing current or voltage feedback control. The established review is presented considering the following main classifications: (a) Number of passive and active power semiconductors; (b) Fault tolerance features; (c) Control complexity; (d) Requirements of specific passive components as capacitor or inductors; (e) Number of independent or split dc-link voltages. Throughout the paper, several specific five-level front-end topologies are presented and comparisons are made between them, highlighting the pros and cons of each one of them as a candidate for the interface of renewable energy sources with the power grid.

1 Introduction

Power converters capable of synthesizing, more than three voltage levels, are commonly classified as multilevel converters, where a common feature is the possibility to deal with higher voltages [1-3]. Mainly due to the required voltage levels in an application, multilevel converters are based on simple structures or based on a cascade connection of simple structures [4-6]. Therefore, approaches with the split dc-link, with multiple dc-links (independently or not), or a mix of both are possible structures that allow synthesizing the multi-voltage levels. Dependent on the application (i.e., interface of renewable energy sources, electric mobility, or storage systems), multilevel converters can be distinguished as active rectifiers, grid-forming or grid-tied inverters, with the possibility, in each case, of using a

voltage-source or a current-source structure. The main objective of a multilevel converter is to synthesize an ac voltage or current with improved quality, also contributing to preserve issues of power quality. Therefore, the key purpose of multilevel converters are to: (a) Deal with semi-conductor limitations in high-voltage applications; (b) Deal with limitations of switching frequency; (c) Improve the power quality; (d) Improve modularity and/or scalability; (e) Deal with controllability [7].

Power quality has been a concern in an electrical grid, however, the interest for this topic has increased along the last decades for both residential and industrial levels [8-11], leading to the development of various multilevel converter topologies [12], as well as control strategies [13]. Moreover, in recent years, due to the advances in semiconductors and digital control platforms, multilevel converters have emerged as a suitable alternative to the conventional static multi-pulse structures (i.e., based on transformers with specific arrangements) as well as an alternative to the conventional two-level converters. The most conventional multilevel converter, i.e., the neutral-point-clamped (NPC), was introduced in the last century and since that date, several proposals were introduced for different applications. Reviews of multilevel converters can be found in [1], in [2], and in [3], where besides the analysis of the topologies in terms of required hardware and software for the control, prospective applications are also included. However, since the publication of these reviews, several multilevel converters have been proposed with innovative features in terms of topology, control, and applications (e.g., considering applications of smart grids, on-grid and off-grid renewable energy sources, electric mobility, microgrids, power transmission, and distribution). Compared to the conventional solutions, increasing the number of voltage levels reduces the size of the passive filters for maintaining similar indices of power quality, consequently allowing to increase the power density of the equipment, which is a key factor in many applications. However, a higher number of levels increases the required hardware resources, which hints to a trade-off between levels, hardware resources, and power density. Based on these criteria, the objective of this paper is not to cover all the multilevel converters, but focusing on five-level converters with the possibility to be applied as grid-tied inverters for interfacing renewable energy sources with the power grid. Therefore, a review of several publications is presented, where the main focus is on voltage-source structures, grid-tied inverters (with current or voltage feedback control), single-phase or three-phase structures, and with five voltage levels. In this context, the main contributions of this paper are related to: (a) The more recent and emerging multilevel converters (five-level) identified in the literature are presented; (b) The multilevel (five-level) converters are organized according to the characteristics; (c) A comparison is established based on the main characteristics in order to identify the pros and cons of each topology.

The paper is directly related with the application of five-level converters to interface renewable energy sources with the power grid, however, the presented topologies can also be useful for other applications, both for coupling with the power grid (i.e., as grid-tied inverters) or for island operation (i.e., as off-grid inverters). A concrete case is the applications of energy storage systems. In fact, the energy storage systems are flexible systems in terms of power operation, which are capable of consuming, storing, or providing energy. Taking into account the flexibility offered, energy storage systems can offer additional advantages for the integration of renewable energy sources, e.g., targeting power management in a distributed architecture. The up-to-date energy storage technologies are compiled and investigated in [14], mainly from the perspective of technology efficiency, maturity, cost, lifespan, and contextualization with the final application scenarios. A review of energy storage systems about problems and challenges for microgrid applications is presented in [15], and past and present of the distinct technologies of energy storage systems are presented in [16]. An overview regarding the history, evolution, and future status of energy storage systems is presented in [17]. Projects directly related to energy storage systems are presented in [18] and [19], while overviews from the power electronics point of view are introduced in [20] and in [21].

The rest of the paper is organized as follows: Section 2 presents an overview of standards for grid-connected converters used for interfacing renewable energy sources; Section 3 presents the selected topologies of five-level front-end converters; Section 4 presents modulation techniques for five-level front-end converters. Section 5 establishes a comparison among the selected topologies; Section 6 ends the paper with the conclusions.

2 Standards for Grid-Connected PV Installations

Over the last decades, the market of PV installations is increasing as a contribution to meet the rising demand. In terms of power, PV installations can vary from few kW to thousands of MW. However, the increased integration of PV-based resources into the power systems can cause diverse effects in practical characteristics that are mainly associated with power quality issues, power management, demand response, reliability, and safety.

Therefore, the integration of photovoltaic (PV) installations must accomplish with specific standards and guidelines, which are established according to the country (i.e., the standards and guidelines can vary from country to country). Such standards are an important requirement, which must be considered in the specifications of the PV installation, as well as in the design of power electronics. The IEEE 1547 and the IEC 61727 are the most widely recognized standards relevant to these applications, which are established by the IEEE (Institute of Electrical and Electronics Engineers) and by the IEC (International Electrotechnical Commission), respectively. Regarding power electronics, the grid-connected front-end converters are designed with the aim to reduce specific harmonic levels, reduce total harmonic distortion (THD), increase power factor, reduce frequency deviation, and eliminate leakage currents.

Summarizing, the IEEE 1547 standard is focused on technical specifications for the interconnection and interoperability among distributed energy resources (DERs) and power systems (at different distribution voltages, emphasizing DER in radial primary and secondary distribution systems) less than 10 MVA. This standard is intended to be universally adopted, where among others, issues such as power quality, safety considerations, islanding, and response to abnormal conditions are addressed. On the other hand, the IEC 61727 standard deals directly with low-voltage non-islanded converters (grid-connected dc-ac inverters). This standard is applied for the interconnection of PV installations (less than 10 kVA) from the power system in the perspective of single-phase or three-phase residences. Regarding the aforementioned standards, Table I summarizes the key points of these standards. Besides the aforementioned standards, there are other relevant standards such as the IEEE 929-2000, which is specific for PV installations with power below 10 kW. This is a recommended practice guidance regarding the interface of PV installations, where there are issues such as power quality, safety, protection, utility system operation, and islanding of PV installations. Other standards, but with lower importance, are established by the NEC, UL, and so on [22-24].

Table I. Summary of the grid requirements concerning the IEEE1547 and IEC 61727 Standards

IEEE 1547		IEC 61727	
Nominal Power	30 kW	10 kW	
	Order	%	Order
Harmonic Level (currents)	3-9	4	3-9
	11-15	2	11-15
	17-21	1.5	17-21

	23-33	0.6	23-33	0.6
	>35	0.3	>35	0.3
	Even harmonics <25% of odd harmonics			
	THD < 5%			
DC current	<1% of rated current		<0.5% of rated current	
Voltage variation	$\Delta V < 50\%$	0.1 s	$\Delta V < 50\%$	0.16 s
	$50\% < \Delta V < 88\%$	2 s	$50\% < \Delta V < 88\%$	2 s
	$110\% < \Delta V < 120\%$	2 s	$110\% < \Delta V < 120\%$	1 s
	$\Delta V > 120\%$	0.05 s	$\Delta V > 120\%$	0.16 s
Frequency variation	$59.3 < \text{Hz} < 60.5$	0.2 s	$59.3 < \text{Hz} < 60.5$	0.16 s

3 Topologies of Five-Level Front-End Converters

In this section, a comprehensive review of the more recent topologies with a special focus on single-phase five-level inverters is provided. It should be noted that the anti-parallel diode of a controlled switch is considered a separate component, as is the case in normal applications.

A five-level three-phase inverter is proposed in [25]; however, the three-phase system consists of three separate phases that can operate individually. In each phase, four fully-controlled power switches and six diodes are needed. This topology is presented in Fig. 1. A coupled inductor is needed for the topology. The output voltage of the converter can be calculated using (1). It should be noted that S_1 operation is complementary to S_2 .

$$V_{out} = \left(\frac{1}{2} (1 - S_2) - S_3 \right) V_{dc} = \left(\frac{1}{2} (1 - S_2) - (1 - S_4) \right) V_{dc} \quad (1)$$

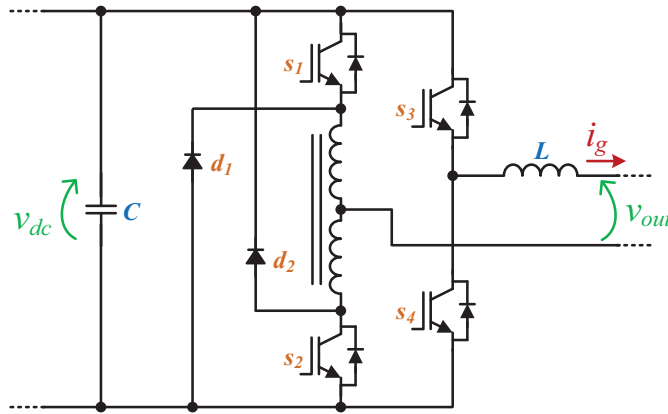


Fig. 1. Topology proposed in [25].

The main advantage of this structure is that it requires fewer controlled switches and has no need for complex voltage control algorithms for dc-link voltage control algorithms as happens with many other topologies. The authors also claim that the topology improves power loss. However, a coupled inductor and certain operating conditions must be met.

In [26] a five-level single-phase inverter based on neutral point and a flying-capacitor is proposed that can produce $\pm v_{dc}/2$, $\pm v_{dc}/4$, and 0. As can be seen in Fig. 2, it has eight fully controlled power switch

and eight diodes. The output voltage of the converter can be calculated using (2). There are multiple alternatives for the $\pm v_{dc}/4$ that can be exploited to maintain the voltage of the floating capacitor within a tight boundary.

$$v_{out} = (S_5 S_6 - S_7 S_8) \frac{v_{dc}}{2} + (S_5 S_7 - S_6 S_8 + S_3 S_4 S_6 - S_1 S_2 S_7) \frac{v_{dc}}{4} \quad (2)$$

It should be noted that the switches and diodes need different voltage ratings, which can increase maintenance costs. Voltage fluctuation in the flying-capacitor can affect output quality, as well as the split power source requirement, which can be limiting, and the utilized switches have different voltage ratings. Moreover, it can only produce half of the total dc-link voltage, which is not desirable. The authors compare the performance of the paper with a commercial NPC-5L topology and the results show a very slight improvement in efficiency.

The authors in [27] modify the structure proposed in [26] and utilize reverse-blocking IGBTs. However, similar to the previous paper, it utilizes the redundant stages to balance the flying-capacitor voltage. The disadvantages are also similar. The authors claim that this topology requires a lower number of semiconductor count, because they are considering each of the reverse blocking IGBTs as one semiconductor. However, a reverse blocking IGBT is in effect composed of two back to back IGBTs that do not have any anti-parallel diode and this advantage is not very prominent. On the other hand, utilizing the reverse blocking IGBTs, improves efficiency. Fig. 2 shows the proposed topology.

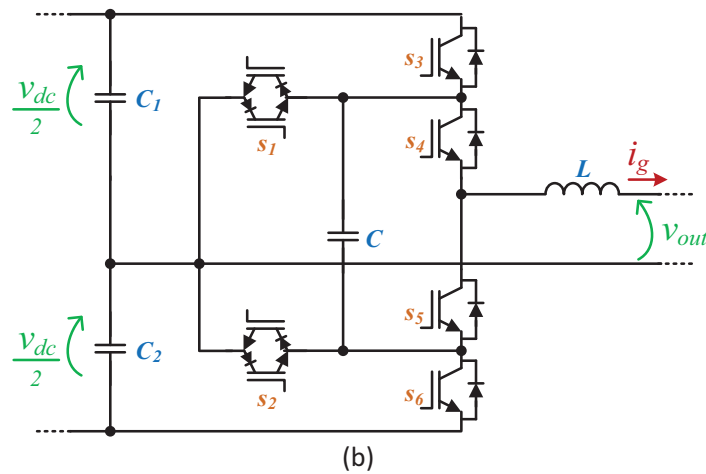
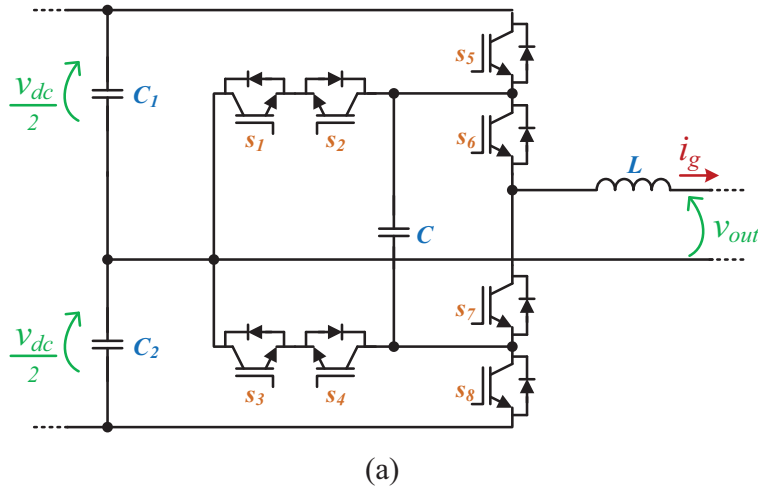


Fig. 2. Topologies: (a) Proposed in [26]; (b) Proposed in [27].

The output voltage of the converter shown in Fig. 2 can be calculated using (3). Comparing (3) with (2), it can be seen that they are essentially similar and the only difference is that [27] (c.f. Fig. 2) utilizes one bidirectional switch instead of two back-to-back unidirectional ones.

$$v_{out} = (S_3 S_4 - S_5 S_6) \frac{v_{dc}}{2} + (S_2 S_4 - S_1 S_5 + S_3 S_5 - S_4 S_6) \frac{v_{dc}}{4} \quad (3)$$

A three-phase five-level topology is proposed in [28]. It requires sixteen controlled switches and sixteen diodes. There are five voltage levels for each phase: $0, v_{dc}/4, 2v_{dc}/4, 3v_{dc}/4, v_{dc}$ that, by considering a three-phase operation would result in nine voltage levels. Although the topology has a relatively low number of switches per voltage levels for all the three-phases, it requires two different sources, where one of them should be a split-voltage source. This topology is presented in Fig. 3. The output phase-voltage of the converter shown in Fig. 3 can be calculated using (4).

$$v_{out} = (S_3 S_6 S_8) \frac{v_{dc}}{2} + (S_1 S_2 S_5 S_7) \frac{3v_{dc}}{4} + (S_1 S_2 S_6 S_7) \frac{v_{dc}}{2} + (S_1 S_2 S_5 S_8) \frac{v_{dc}}{2} \quad (4)$$

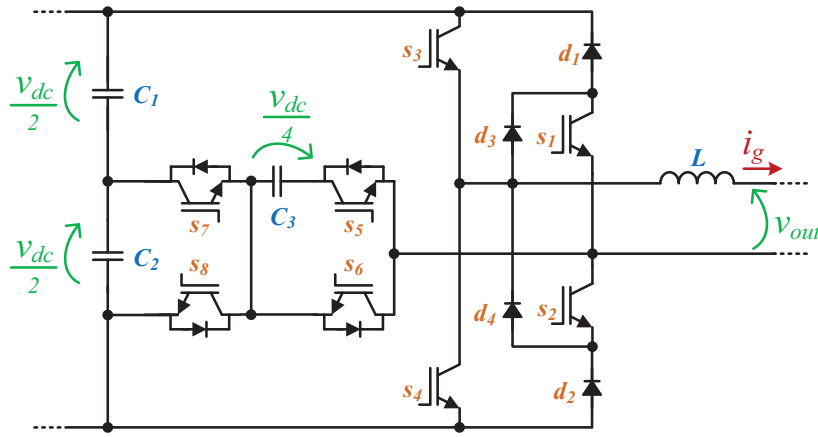


Fig. 3. Topology proposed in [28].

Authors in [29] utilize a seven-level converter previously proposed by Kamal Al-Hadad called PUC to build a five-level converter with simplified control. This topology is presented in Fig. 4. It is argued that the previously proposed seven-level converter has a very complex control and requires a high switching frequency as well as additional sensors. However, the simplified five-level converter changes the ratio $V_1=3V_2$ to $V_1=2V_2$ and also introduces a self-balancing algorithm to simplify the control. The output voltage levels are $\pm v_{dc}/2, \pm v_{dc}/4, 0$, which achieve a unity voltage ratio between output to the input voltage. The unnecessary of a split power source is another advantage of such a system. The output phase voltage of the topology shown in Fig. 4 can be calculated based on the switch states using (5).

$$v_{out} = (S_1 S_5 S_6 - S_2 S_3 S_4) \frac{v_{dc}}{2} + (S_1 S_3 S_5 + S_1 S_2 S_6 - S_3 S_4 S_5 - S_2 S_4 S_6) \frac{v_{dc}}{4} \quad (5)$$

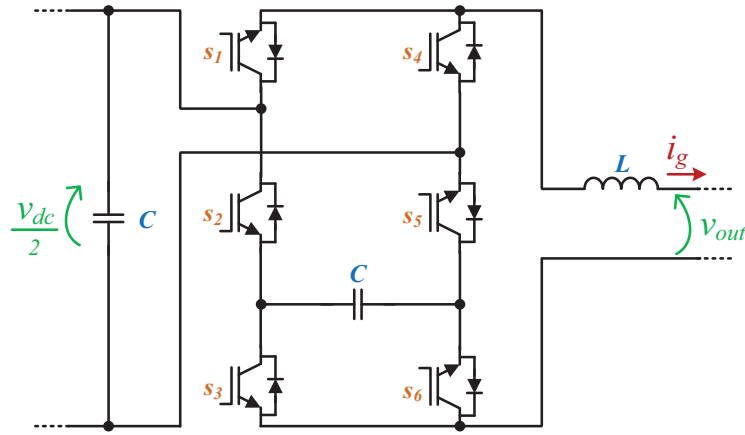


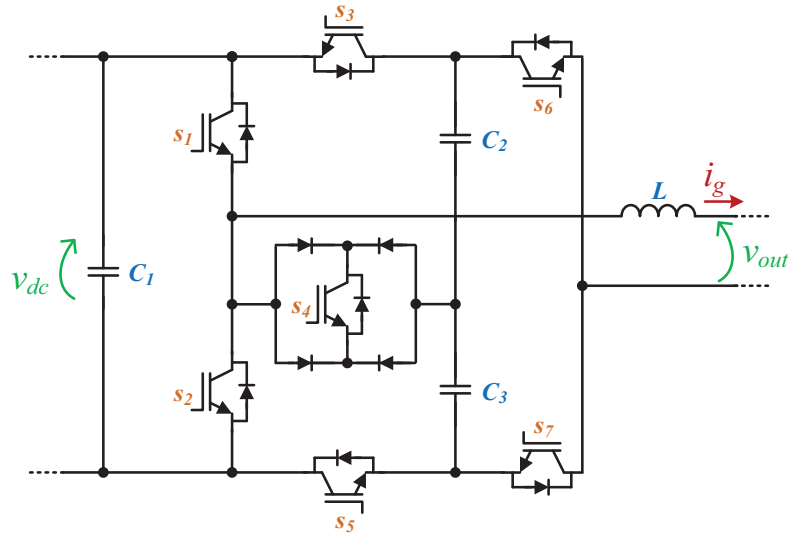
Fig. 4. Topology proposed in [29].

A single-phase five-level structure is proposed in [30] based on the switching capacitor technique. Fig. 5(a) shows the proposed structure and the phase output voltage can be calculated using (6). Since the capacitors utilized in the topology can be easily balanced without needing any complex closed-loop control, one of the advantages of this system is a simple control. However, the most important benefit of the presented circuit is its voltage boosting capability. For an input source with a voltage v_{dc} , it can produce a five-level ac output voltage with voltage levels of $0, \pm v_{dc}$, and $\pm 2 v_{dc}$. For achieving this goal, one power supply, two capacitors, ten diodes, and seven power switches are required. This structure has a high number of active and passive components; however, one main advantage of this method is that it can produce an output twice the voltage level of the power supply.

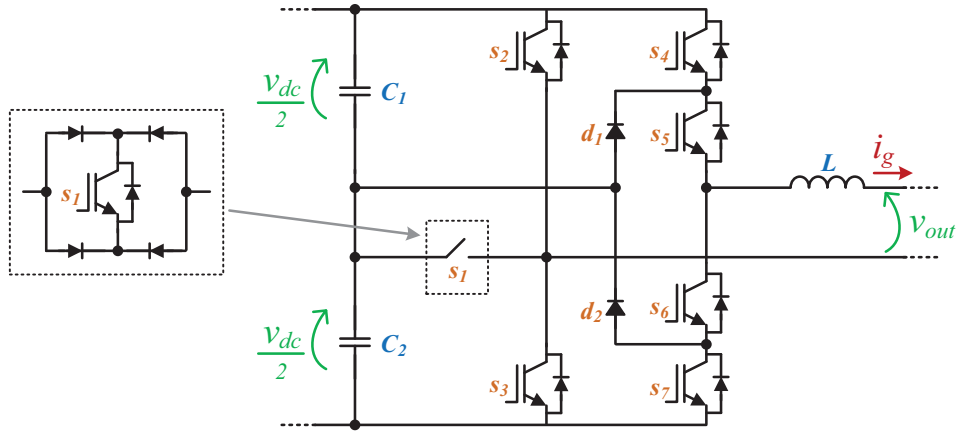
$$v_{out} = (S_1 S_7 - S_2 S_6)2v_{dc} + (S_1 S_4 S_5 S_7 + S_2 S_3 S_4 S_7 - S_1 S_4 S_5 S_6 - S_2 S_3 S_4 S_6)v_{dc} \quad (6)$$

In [31], a single-phase five-level inverter with fault tolerance is proposed. The proposed converter consists of seven power switches as well as twelve power diodes. A diode-bridge in combination with a power switch in the output is utilized to cut-off the fault current. However, the utilized diode bridge of the fault circuit breaker in the output can severely hinder the efficiency of the converter. Fig. 5(b) shows the structure of the converter proposed in [31]. The output voltage of the topology shown in Fig. 5(b) can be calculated based on (7), while S_7 can be used for interrupting the current path during faults.

$$v_{out} = (S_3 S_4 S_5 - S_2 S_6 S_7)v_{dc} + (S_3 S_5 S_6 - S_2 S_5 S_6)\frac{v_{dc}}{2} \quad (7)$$



(a)



(b)

Fig. 5. Topologies: (a) Proposed in [30]; (b) Proposed in [31].

A five-level inverter with a modular switched capacitor circuit is proposed in [32]. The main advantage of this topology is that the voltage levels can be increased by adding more switched capacitor bridge modules. As can be seen in Fig. 6, the topology has twelve diode-switch sets for a five-level inverter. With each extra switched capacitor module, the output voltage amplitude can be increased to four times the input voltage v_{dc} . The first two switching groups are defined by (8) and (9).

$$S_P = S_3 S_7 S_9 S_{10} \quad (8)$$

$$S_N = S_4 S_6 S_8 S_{11} \quad (9)$$

Considering the defined switching groups and the remaining switches, it is possible to calculate the output phase voltages, according to (10). It should be noted that the S_P and S_N are complementary.

$$v_{out} = (S_P + S_N)[(S_2 S_5 - S_1 S_6)4v_{dc} + (S_2 S_6 - S_1 S_5)2v_{dc}] \quad (10)$$

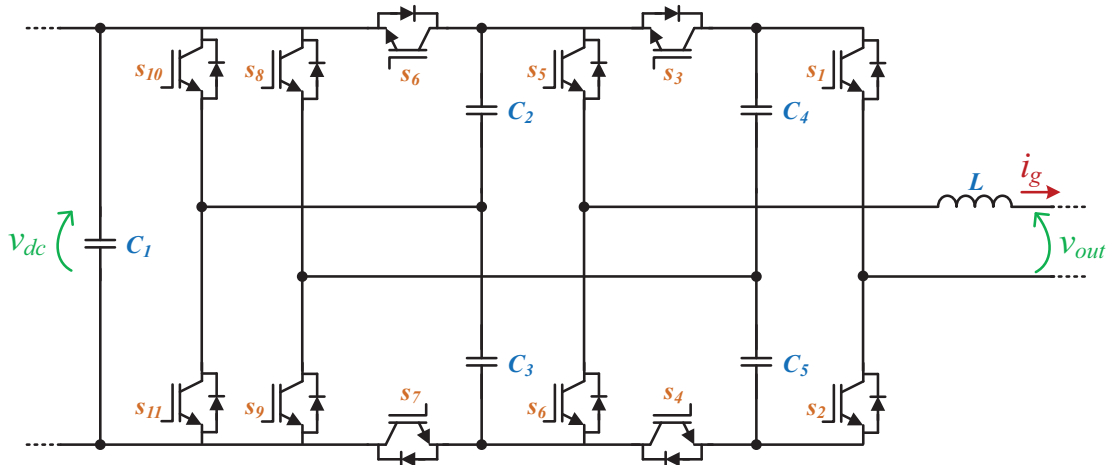


Fig. 6. Topology proposed in [32].

Another five-level fault-tolerant structure is proposed in [33]. This topology is presented in Fig. 7. It consists of six IGBT-diode sets, as well as a bidirectional switch and an NPC leg. Compared to many other topologies with fault current limiting capability, this one has a moderate number of switches and capacitors. The required NPC can be considered one of the disadvantages of such topologies. Moreover, this topology can produce output voltages in the range of $\pm v_{dc}$. The output voltage levels based on the input source and the capacitor voltage can be calculated using (11). In the case of $v_{c2} = v_{dc}/2$ there are five symmetrical voltage levels.

$$v_{out} = (S_1 S_2 S_6 - S_3 S_4 S_5)v_{dc} + (S_1 S_2 S_7 + S_2 S_3 S_7)(v_{dc} - v_{c2}) - (S_3 S_4 S_7 + S_2 S_3 S_5)v_{c2} \quad (11)$$

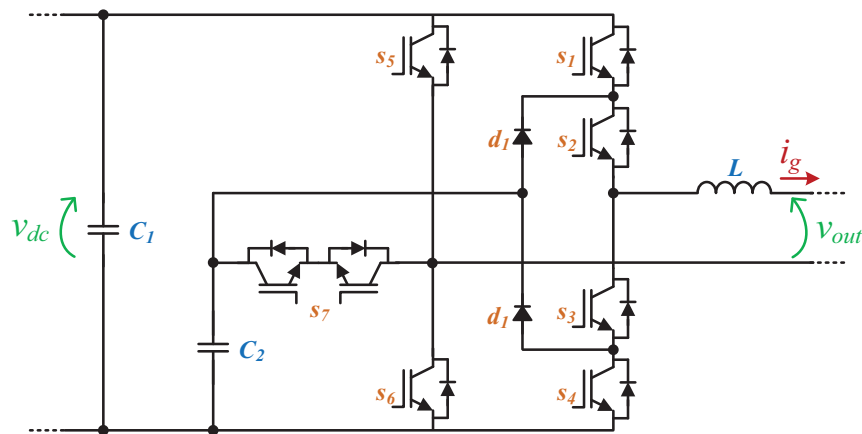


Fig. 7. Topology proposed in [33].

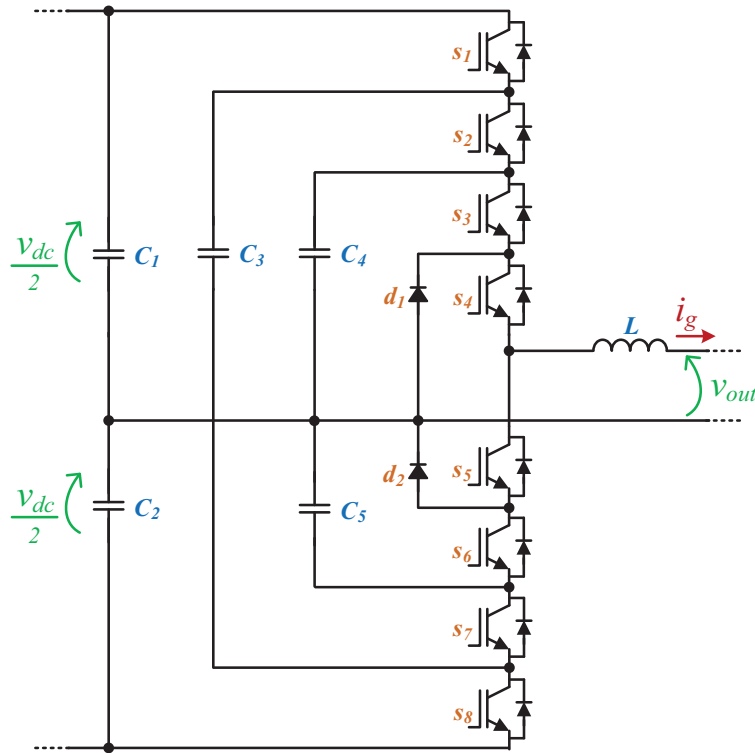
A five-level inverter for medium voltage applications is proposed in [34]. Although the paper focuses on a three-phase structure, it can be easily utilized as a single-phase system too. The system includes eight switch-diode sets as well as two extra diodes for each phase. One of the disadvantages of such a topology is requiring a split-source supply and three additional capacitors. The output voltage levels include: $v_{dc}/2$, $v_{dc}/4$, 0, $-v_{dc}/4$, $-v_{dc}/2$. Fig. 8(a) shows the above-mentioned topology. Another

disadvantage of this topology is a relatively complex balancing procedure for the three flying-capacitors in each phase. Although the authors claim that the number of diodes is reduced compared to many previous topologies, the number of semiconductor devices is still relatively high. The output phase voltage of the topology shown in Fig. 8(a) can be calculated based on the switch states using (12).

$$v_{out} = (S_1 S_2 S_3 S_4 - S_5 S_6 S_7 S_8) \frac{v_{dc}}{2} + (S_1 S_2 S_4 S_5 + S_2 S_3 S_4 S_8 + S_1 S_3 S_4 S_7 - S_4 S_5 S_7 S_8 - S_1 S_5 S_6 S_7 - S_2 S_5 S_6 S_8) \frac{v_{dc}}{4} \quad (12)$$

Fig. 8(b) depicts another five-level inverter based on a split-source supply [35]. It requires fourteen switch-diode sets and four extra diodes. Although this topology requires a higher number of semiconductor devices compared to the topology proposed in [34], it has some other significant advantages including: simpler control, no flying-capacitor, and fault-tolerant structure. The output voltages are: $-v_{dc}$, $-v_{dc}/2$, 0 , $v_{dc}/2$, v_{dc} , which can be calculated using (13).

$$v_{out} = (S_1 S_2 S_7 S_8 - S_3 S_4 S_5 S_6) v_{dc} + (S_1 S_2 S_6 S_7 + S_2 S_3 S_7 S_8 - S_2 S_3 S_6 S_7 - S_3 S_4 S_6 S_7) \frac{v_{dc}}{2} \quad (13)$$



(a)

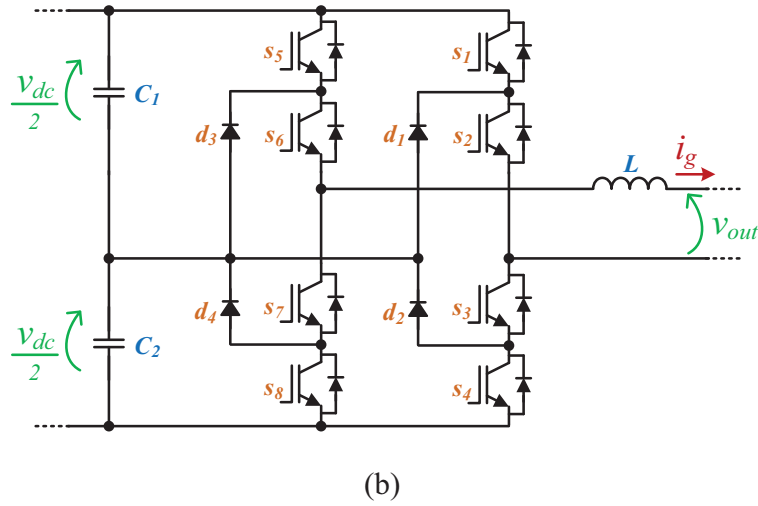


Fig. 8. Topologies: (a) Proposed in [34]; Proposed in [35].

A bidirectional topology based on a half-bridge front-end structure and two flying-capacitor cascade structures is proposed in [36]. This topology is shown in Fig. 9. This topology has a split dc-link and two flying-capacitors, which represents the main disadvantage of this topology since it increases the control complexity. When compared with other topologies, this one requires a significative number of switching devices. Each of the flying-capacitor cells is formed by four switching devices, which are responsible for producing three voltage levels. The output phase voltage of the topology shown in Fig. 9 can be calculated based on the switch states defined in (14).

$$v_{out} = (S_1 S_3 S_4 - S_2 S_9 S_{10}) \frac{v_{dc}}{2} + (S_1 S_3 S_6 + S_1 S_4 S_5 - S_2 S_8 S_9 - S_2 S_7 S_{10}) \frac{v_{dc}}{4} \quad (14)$$

In this case, the following switches work in a complementary manner.

$$\begin{aligned} S_5 &= 1 - S_3 \\ S_4 &= 1 - S_6 \\ S_7 &= 1 - S_9 \\ S_8 &= 1 - S_{10} \\ S_1 &= 1 - S_2 \end{aligned} \quad (15)$$

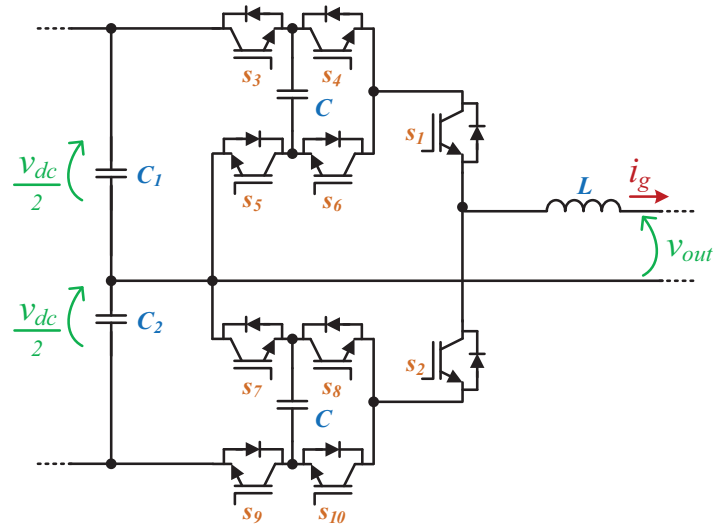


Fig. 9. Topology proposed in [36].

A bidirectional topology based on a full-bridge front-end structure and a bidirectional-bipolar cell connected between the neutral wire and a split dc-link is presented in [37]. This topology is presented in Fig. 10(a). The full-bridge structure is responsible for obtaining three voltage levels ($+v_{dc}$, 0 , $-v_{dc}$), while the bidirectional-bipolar cell is responsible for obtaining the other two voltage levels ($+v_{dc}/2$, $-v_{dc}/2$). The output phase voltage can be calculated using (16). In order to optimize the efficiency, the switching devices S_1 and S_2 can be switched at a low-frequency (i.e., the frequency of the power grid voltage), while the other switching devices are switched at high-frequency.

$$v_{out} = (S_2 S_3 - S_1 S_4)v_{dc} + (S_3 S_5 - S_4 S_5)\frac{v_{dc}}{2} \quad (16)$$

A bidirectional topology based on a full-bridge front-end structure and a back-end dc-dc structure with a split dc-link is presented in [38]. This topology, shown in Fig. 10(b), operates with five voltage levels, according to the operation of the back-end dc-dc converter. The switching devices s_1 and s_2 are switched at a low-frequency (i.e., the frequency of the power grid voltage), while the other switching devices are switched at high-frequency. As claimed in the paper, this is an important aspect since it is possible to optimize the operation of the converter, reducing the switching losses. The output phase voltage of the topology shown in Fig. 10(b) can be calculated based on the switch states using (17).

$$v_{out} = (S_2 S_3 S_7 S_8 - S_1 S_4 S_7 S_8)v_{dc} + (S_2 S_3 S_6 S_7 - S_1 S_4 S_5 S_8)\frac{v_{dc}}{2} \quad (17)$$

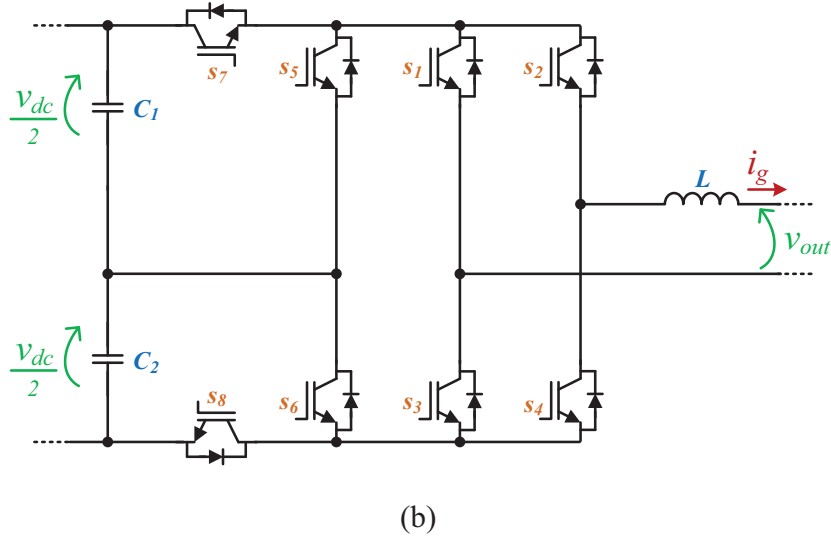
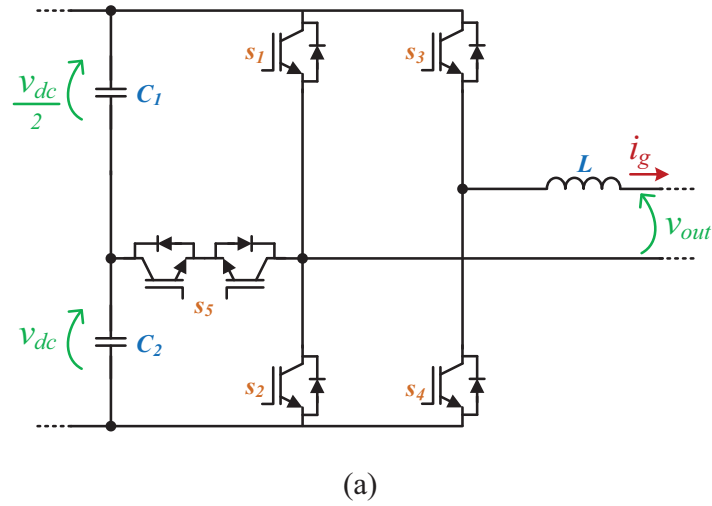


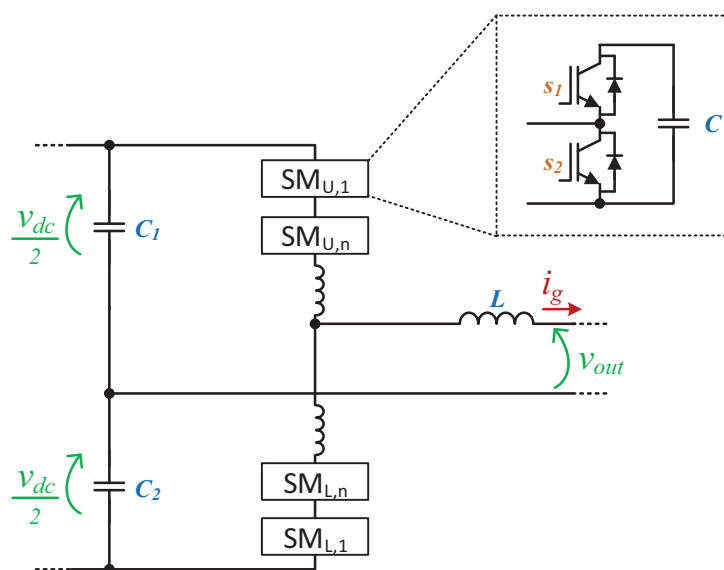
Fig. 10. Topologies: (a) Proposed in [37]; (b) Proposed in [38].

Modular multilevel converters (MMC) are another type of circuit that can realize five-level output voltage [39, 40]. In a way, MMCs are an extension of the earlier multilevel circuits based on the flying-capacitors, with the exception that MMCs are much more feasible in higher voltage levels [41]. Theoretically, there is no limit to the number of voltage levels that an MMC can achieve, but the practical considerations such as controller complexity and cost would limit the number of voltage levels. Since the main advantage of the MMC topologies is in higher voltage and higher voltage levels, here only two of the more basic topologies that utilize half-bridge and full-bridge submodules are considered that are shown in Fig. 11(a), Fig. 11(b), and Fig. 11(c). The output voltage of the submodules shown in Fig. 11(a), Fig. 11(b), and Fig. 11(c), can be calculated using (18), (19), and (20), respectively.

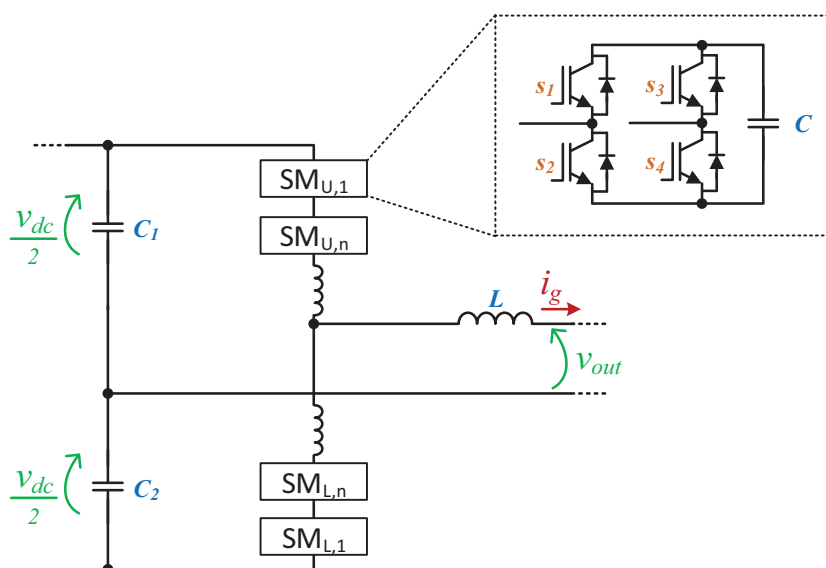
$$v_{SM} = (1 - S_2)v_C \quad (18)$$

$$v_{SM} = (S_1 S_4 - S_2 S_3)v_C \quad (19)$$

$$v_{SM} = (S_1 S_3 S_6 S_8 - S_2 S_4 S_5 S_7)v_C \quad (20)$$



(a)



(b)

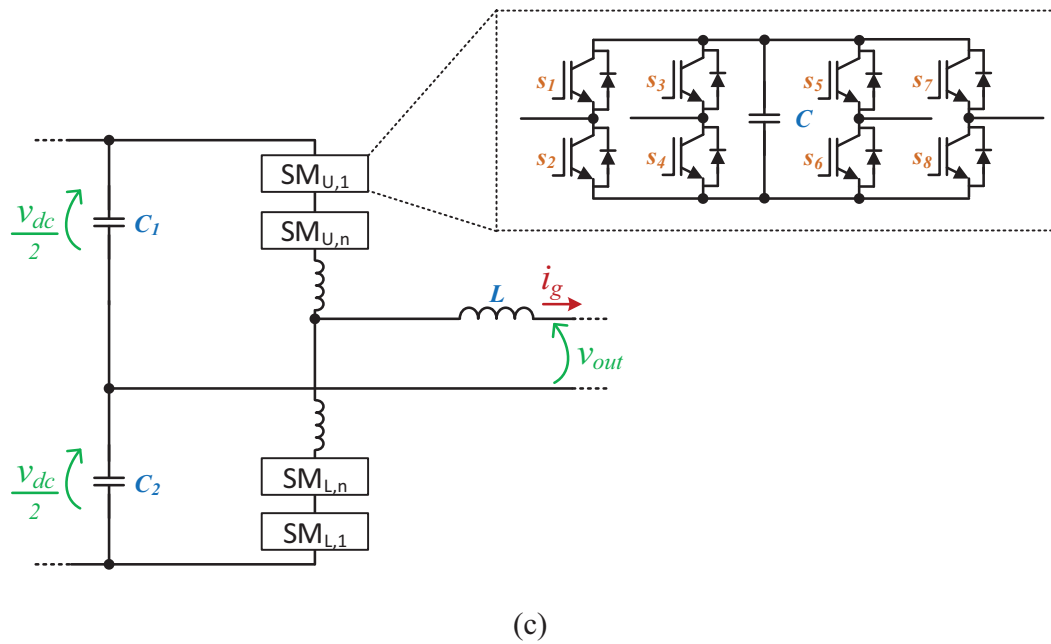


Fig. 11. MMC topologies: (a) Proposed in [42]; (b) Proposed in [43]; (c) Proposed in [44].

In [42] each MMC submodule has a half-bridge structure requiring two switches and two diodes. With the structure proposed in [42], eight switch-diode sets, two inductors, and four capacitors are required [45]. However, it is possible to reduce the number of required modules to half, if the switching technique in [46] is utilized. Based on the control technique proposed in [46], four switch-diode sets, two inductors, and four capacitors are required. On the other hand, the size of the required inductor increases. The structure proposed in [43], requires double the switch-diodes sets, than the one proposed in [42]; however, because of the control proposed in [43], smaller capacitors can be used, while at the same time increase the output to input voltage ratio to around $0.7v_{dc}$. Another advantage of these MMCs is better fault tolerance.

There are other MMC topologies that focus on additional features such as sensorless balancing and/or parallel connection [39, 45, 47, 48]. As an example, an extra half-bridge is introduced in [44, 49] that brings about the capability to connect neighboring modules in parallel. The parallel connection decreases string impedance, reduces current ripple, and improves the balancing capability of the capacitors. The parallel connection of modules distributes load current among multiple capacitors [50] and reduces requirements on the current rating of the switches to one half. Sizing the switches to lower current ratings compensates double the number of discrete switches of the MMCSP, and the amount of silicon needed is comparable to the MMC topology in [43]. The control method proposed in [51] reduces the complexity of the control algorithm to the level of standard MMCs. Large voltage differences and temporal imbalance might cause inrush currents between paralleled modules and reduce the feasibility of the parallel mode. Means to overcome the inrush currents are presented in [47].

4 Modulation Techniques for Five-Level Front-End Converters

One distinguishing aspect of the multilevel converters, when compared to the traditional two-level converters, is the wide variety of usable modulation techniques. Multilevel converters require different modulation techniques in order to synthesize all its possible voltage levels, regardless of being three-level, five-level, or higher-level converters. Moreover, different modulation techniques can be applied to the same converter, as is the case of the most traditional techniques, but some techniques are

only feasible to specific converters, as is the case of techniques that are specially developed for a given converter in order to optimize, for instance, the switching losses.

In a voltage source inverter, the modulation technique is responsible for transforming a given reference voltage into a set of defined states of the switching devices comprising the converter, so that the desired reference voltage or current, depending on the used feedback control, is produced at its ac side. The two most common groups of modulation techniques for voltage source inverters, regardless of the number of voltage levels, are the pulse-width modulation (PWM) and the space vector modulation (SVM). However, these two groups of modulation techniques must be properly adapted when applied to multilevel converters.

4.1 Pulse-Width Modulation (PWM)

PWM is a modulation technique widely used in two-level and three-level inverters, where a single triangular carrier and one (in two-level inverters) or two (in three-level inverters) reference voltages are used. The popularity of this technique is due to its ease of implementation, especially regarding digital signal processor (DSP) based control systems, and due to the establishment of a fixed switching frequency, which is useful for sizing the output passive filters of the converter. Besides, since most inverters contain complementary pairs of active switches, one triangular carrier can be used to generate a pair of complementary signals for the switches. However, in multilevel converters, it is mandatory to use either more than one triangular carrier or more than two reference voltages in order to obtain the total number of possible voltage levels.

The classical multilevel PWM techniques consist of increasing the number of triangular carriers, which are either vertically or horizontally distributed, and the number of triangular carriers must be $n-1$, where n is the number of voltage levels. For the specific case of this paper, i.e., five-level inverters, four triangular carriers and one reference voltage should be used in order to attain a five-level operation with a classical multilevel PWM technique. Besides, taking into consideration the triangular carriers disposition, two main schemes can be feasible, i.e., with vertical disposition and horizontal disposition. In a vertical disposition-based PWM, all the carriers have the same amplitude and frequency but different average values, so that the maximum value of a given carrier coincides with the minimum value of the upper one, and so on. In this case, two of the carriers are only positive and the other two are only negative. In terms of phase, there are three main approaches regarding vertical-disposition PWM schemes: (a) phase disposition, where all the carriers have the same phase (Fig. 12(a)); (b) phase opposition, where the positive carriers are 180° phase shifted with the negative carriers (Fig. 12(b)); (c) alternative phase opposition, where the consecutive carriers are 180° phase shifted from each other (Fig. 12(c)). Vertical-disposition is suitable for topologies comprising a split dc-link, such as NPC and flying-capacitor, but can lead to power unbalances in topologies with independent dc-links. Regarding horizontal-distribution, this scheme is also termed as phase shifted PWM, where all the carriers have the same amplitude, average value and frequency but different phase angles. The phase shift between consecutive carriers should be equal to $360^\circ/n$, where n is the number of triangular carriers. Hence, in this case, each triangular carrier is 90° phase shifted from each other, as can be seen in Fig. 12(d). Another possibility is to use two reference voltages 180° phase shifted between each other (as in a unipolar PWM scheme) and only two triangular carriers obeying to a $180^\circ/n$ ratio. In this case, the carriers are not evenly divided in one switching period due to the additional reference voltage, which emulates the two removed carriers, as can be seen in Fig. 12(e). Horizontal-disposition schemes have the advantage of multiplying the switching frequency (the frequency of each carrier) into the output frequency by a factor of n , (four, in this case), similarly to an interleaved converter. Compared to vertical-disposition, this scheme allows a balanced power distribution in topologies such as cascaded

multilevel and a natural voltage balancing in the flying-capacitor topology. Nevertheless, vertical-distribution schemes allow a lower THD in the output voltage than the horizontal-distribution for the same characteristics of operation [3, 52-56].

However, depending on the available resources, the use of multiple triangular carriers can also be an obstacle. One method to suppress this is to use a single triangular carrier but different reference voltages, also called modified reference voltages. Therefore, each complementary pair of signals for the active switches is achieved not from each triangular carrier but from each reference voltage. This approach can also be used to optimize the switching frequency of a multilevel converter. For instance, in [38] is implemented a modulation strategy that allows an active switch pair to operate with a switching frequency equal to the low-frequency component of the output voltage, i.e., the power grid frequency. This allows reducing the switching losses of the converter or, even further, to apply a different type of power semiconductor that does not need to be fully-controlled (e.g., thyristor), offering lower conduction losses and a lower cost. Fig. 12(f) shows an example of this modulation scheme, where one carrier and two references can be seen, generating three pairs of switch signals.

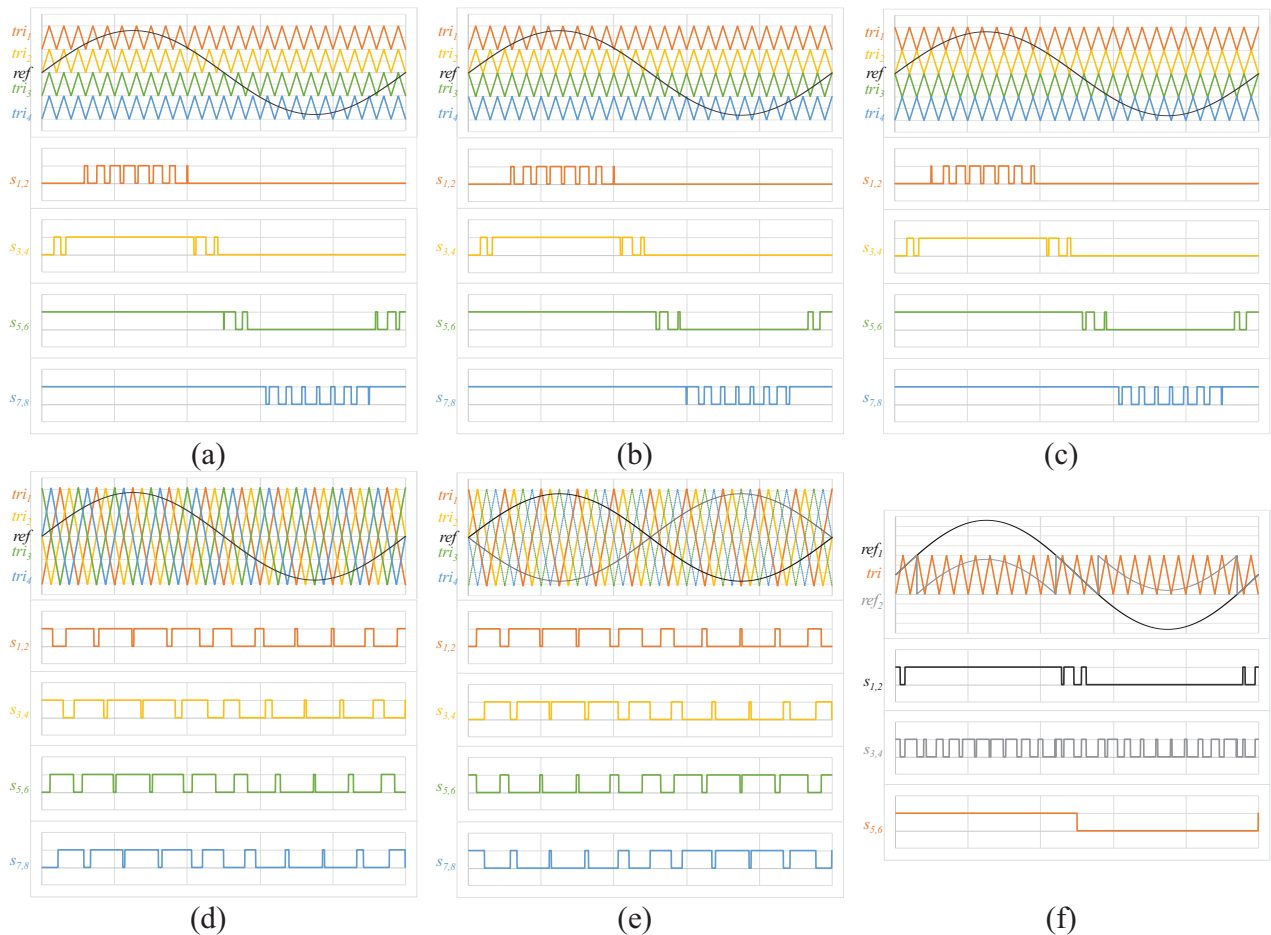


Fig. 12. Pulse-width modulation: (a) Vertical phase disposition PWM carriers for five-level inverters; (a) Vertical phase opposition PWM carriers for five-level inverters; (c) Vertical alternative phase disposition PWM carriers for five-level inverters; (d) Horizontal disposition PWM carriers for five level inverters using based on four carriers and one reference voltage; (e) Horizontal disposition PWM carriers for five level inverters using based on two carriers and two reference voltages; (f) Horizontal-disposition PWM carriers for five-level inverters using a single carrier and a modified reference voltage.

4.2 Space Vector Modulation (SVM)

While the PWM techniques are based on the modulation of each complementary pair of active switches, the SVM technique consists of acting upon the converter as a whole. This means that, in each instant, the state of all the active switches comprising the converter is determined in order to satisfy a given reference voltage. This is achieved via a coordinate transformation from $a-b-c$ to $\alpha-\beta$, where the reference frame is divided into sectors that contain a given output voltage. In order to synthesize the desired voltage (which is contained in a given sector), two adjacent voltage vectors (which are produced by a given converter state) should be used, with the length of each one being proportional to the on-time of each converter state. Compared to PWM, SVM also allows a fixed switching frequency, but reduces the total number of commutations of a given switch in each output cycle, since each switch state can be assigned in a way that avoids redundant switching. A similar strategy, called pulse decoding, can be seen in [57], where only one switch pair switches at high-frequency. Moreover, SVM allows a better utilization of the dc-link voltage, since it inherently comprises a third harmonic injection that allows achieving an output voltage 15% higher than PWM for the same dc-link voltage and modulation index. Due to this reason, SVM is an interesting modulation technique to be applied in three-phase inverters for three-wire systems, as is the case of traction applications, for instance [58, 59]. The main disadvantage of SVM compared to PWM is its complexity, requiring calculations that do not exist in PWM.

In multilevel converters, SVM is attainable through a higher number of sectors, as well as a higher number of voltage vectors. While three-phase two-level converters allow six non-null voltage vectors and six sectors, as can be seen in Fig. 13(a) three-phase five-level converters allow sixty non-null and non-redundant voltage vectors, comprising a total of ninety-six sectors, as represented in Fig. 13(b). each triangle represents a sector, while each triangle vertex represents one voltage vector. The number of voltage vectors depends on the nature of the converter, i.e., whether it allows redundant states (multiple voltage vectors to produce the same output voltage) or not (only one voltage vector to produce a given output voltage) [60-62]. SVM is advantageous over PWM when the number of levels is very high, i.e., when controlling the converter as a whole is simpler to implement instead of controlling each complementary switch pair.

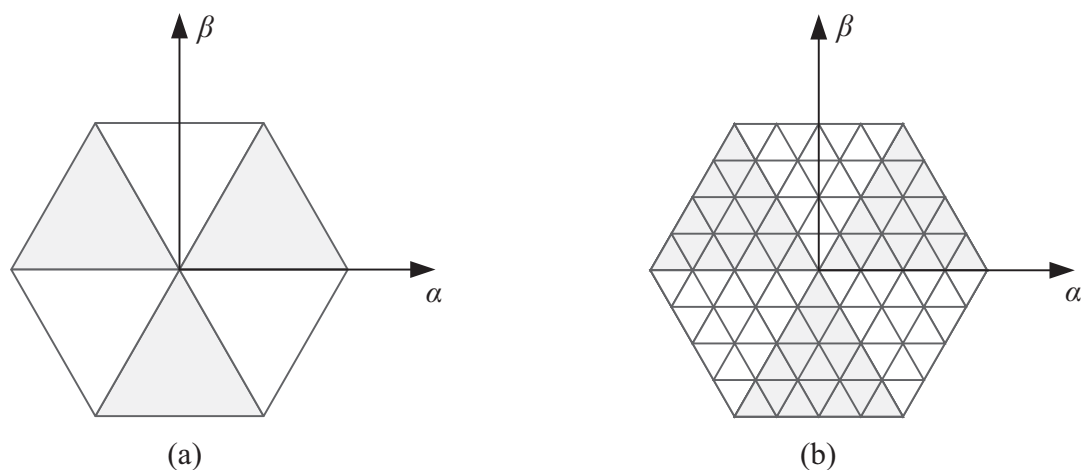


Fig. 13. Space vector representation for three-phase inverters: (a) Two-level; (b) Five-level.

5 Comparison between Topologies

This section presents a comparison regarding the topologies identified in section 3. The comparison was performed considering three main categories: with flying-capacitor, without flying-capacitors, and MMCs. For all the topologies, the key parameters were considered. Table II shows the comparison between the topologies. Analyzing this table in more detail, the MMC topologies [44, 49] requires more devices (diodes and switching devices), which can be identified as a disadvantage since it can increase the conduction and switching losses, contributing to reduce the efficiency. Besides the MMC topologies, the topology [28] requires two sources and is the only topology with this requisite, which can be impeditive for applications as renewables since two independent sources are required. The topology [25] requires the use of a transformer, which can be a disadvantage, but it only requires a single source and no capacitors for obtaining the five voltage levels. Topologies [25, 29, 30, 32, 33] require a single dc-link, i.e., it is not necessary a split dc-link for the operation with five-levels, therefore, for applications as renewables, this is an interesting aspect. Since fault tolerance and reliability issues are not the main focus of this review, only a few examples of the more recent topologies [31, 33, 43] were considered. Considering the fault-tolerant topologies, it is clear that higher tolerance to fault comes at the cost of a significantly higher number of active components.

The main problem in the methods based on the flying-capacitors is the control complexity. When the capacitor voltage is a fraction of the supply voltage, then the controller should monitor the voltage of that capacitor and actively maintain it in a tight boundary. On the other hand, the methods based on the multiple/split sources are more expensive to implement in the end, since they require either separate power sources or keeping the split source voltage considering all the inherent differences in the system. The capacitors of the split dc-link may exhibit a difference in voltage sharing, causing a voltage ripple in the dc-link. Consequently, the stabilization of the voltage ripple may require a considerably large dc-link capacitor. In addition, any imbalance in the load causes a neutral current, which causes a perturbation in the split dc-link voltage [63]. Consequently, balancing the split dc-link capacitors is the subject of a proper control. Therefore, as happens always in engineering applications, here a trade-off should be maintained on the control complexity, sensor requirements, fault tolerance, and cost. Regarding the topologies based on modular structures, only a few of them are present, since the main advantage of such methods are framed in higher voltage levels. Therefore, as a five-level converter, modular multilevel methods are not very economical.

Regarding the number of semiconductors, it is commonly known that a higher number of passive semiconductors contributes to decrease the cost and the control complexity of the inverter, but negatively affects its efficiency [64]. Consequently, the additional production of heat contributes to increase the requirements on system cooling, as well as to accelerate the aging of semiconductors [65]. In this context, higher efficiency is generally achieved by trading the number of passive semiconductors (e.g., diodes) and active semiconductors (e.g., MOSFETs and IGBTs) [66]. Naturally, a higher overall number of components in the inverter, both passive and active, lowers its reliability, if the components do not introduce fault-tolerance itself [67].

Table II. Comparison between the presented topologies.

Category	Reference	Number of Switches ⁽¹⁾	Number of Diodes	Number of Sources	Number of Caps	Needs Split dc-link	Number of Inductor	$V_{out,max}/V_{in}$	Output Voltage Levels	Control Complexity	Fault Tolerant
With Flying-Capacitors	[26]	8n	8n	1	n	Yes	0	$1/2$	$\pm v_{dc}/2, \pm v_{dc}/4, 0$	***	No
	[27]	8n	6n	1	n	Yes	0	$1/2$	$\pm v_{dc}/2, \pm v_{dc}/4, 0$	***	No
	[29]	6n	6n	1	n	No	0	1	$\pm v_{dc}, \pm v_{dc}/2, 0$	**	No
	[30]	7n	10n	1	2n	No	0	2	$\pm 2v_{dc}, \pm v_{dc}, 0$	**	No

Without Flying-Capacitors	[32]	12n	12n	1	4n	No	0	4	$\pm 4v_{dc}, \pm 2v_{dc}, 0$	**	No
	[34]	8n	10n	1	3n	Yes	0	1/2	$\pm v_{dc}/2, \pm v_{dc}/4, 0$	***	No
	[36]	10n	10n	1	2	Yes	0	1	$\pm v_{dc}, \pm v_{dc}/2, 0$	***	No
	[25]	4n	6n	1	0	No	1	1	$\pm v_{dc}, \pm v_{dc}/2, 0$	*	No
	[28]	4n+4	4n+4	2	0	Yes	0	1	$\pm v_{dc}, \pm 3v_{dc}/4, \pm v_{dc}/2, \pm v_{dc}/4, 0$	*	No
	[31]	7n	10n	1	0	Yes	0	1/2	$\pm v_{dc}/2, \pm v_{dc}/4, 0$	*	Yes
	[33]	8n	8n	1	0	No	0	1	$\pm v_{dc}, \pm v_{dc}/2, 0$	***	Yes
	[35]	14n	18n	1	0	Yes	0	1	$\pm v_{dc}, \pm v_{dc}/2, 0$	***	Yes
	[37]	5n	9n	1	0	Yes	0	1	$\pm v_{dc}, \pm v_{dc}/2, 0$	**	No
	[38]	8n	8n	1	0	Yes	0	1	$\pm v_{dc}, \pm v_{dc}/2, 0$	**	No
Modular Methods	[42]	8n	8n	1	4	Yes	2	0.5	$\pm v_{dc}/2, \pm v_{dc}/4, 0$	***	No
	[43]	8n	8n	1	2	Yes	2 ⁽²⁾	0.71	$\pm v_{dc}, \pm v_{dc}/2, \pm v_{dc}/4, 0$	***	Yes
	[46]	4n	4n	1	2	Yes	2 ⁽²⁾	0.5	$\pm v_{dc}/2, \pm v_{dc}/4, 0$	***	No
	[44, 49]	16n	16n ⁽³⁾	2	2	Yes	2	1	$\pm v_{dc}, \pm v_{dc}/2, 0$	**	Yes

(1) Anti-parallel diodes of the IGBTs are considered separate components, as is the case in many applications

(2) relatively large inductors

(3) with half the rated current on each switch

6 Conclusions

Worldwide, distributed renewable energy resources are seen as absolutely fundamental to accomplish with the target to minimize environmental concerns, to obtain access to affordable energy, and to contribute to a sustainable power grid. Over the past few decades, in order to enable the increasingly effective integration of renewable energy sources, power electronics technologies have played a leading role. In fact, even today, power electronics technologies are seen as one of the fundamental challenges for the widespread use of renewable energy sources. Embracing this context, this paper presents a review of power electronics converters that can be used for interfacing renewable energy sources into the power grid, concentrating on front-end converters with a voltage-source structure. More specifically, in a more attractive future perspective, this review is only focused on five-level structures. Thus, throughout the paper, the most relevant five-level topologies for the contextualization of renewable energy sources in smart grids are presented. As result, an effective comparison between the topologies is presented, highlighting key aspects that are useful to select a topology in detriment of others, according to the number of passive and active semiconductors, sources, capacitors, split dc-links, inductors, and voltage levels. As an example, based on the established comparison, it is possible to conclude that topologies with more than one source are not advantageous and, on the other hand, topologies with a single dc-link represent an interesting aspect for renewable energy source applications. Based on the established comparison, it is possible to conclude that topologies with more than one source are not advantageous and, on the other hand, topologies with a single dc-link represent an interesting aspect for renewable energy source applications. The comparison also shows that topologies with a flying capacitor are not ideal concerning fault-tolerant characteristics, and it was identified a topology that accomplishes with the combined criteria as fault-tolerant, unnecessary of flying capacitors, and with reduced control complexity, which are three relevant features for obtaining reliable and high-efficiency converters to interface renewable energy sources with the power grid. The topologies that require lower control complexity are all based on structures independent of flying capacitors, which is understandable, since such capacitors require a dedicated control loop. Moreover, such topologies require additional hardware, such as sensors and signal conditioning circuits. On the other hand, the topologies based on modular structures require more control complexity, since these structures are based on submodules (i.e., constituted by half-bridge or full-bridge converters). Notwithstanding, it is important to emphasize that the objective of this paper is not directly related to the identification of a specific topology that complies with all the benefits under study; it has the goal

of presenting the different advantages and disadvantages of each topology in order to facilitate the comparison of such topologies for different purposes.

7 Conflict of Interest

The authors declare no conflict of interest.

8 References

- [1] A. Pandey, B. Singh, B. N. Singh, A. Chandra, K. Al Haddad, and D. P. Kothari, "A review of multilevel power converters," *Journal of the Institution of Engineers (India): Electrical Engineering Division*, vol. 86, no. MAR., pp. 220-231, 2006.
- [2] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE transactions on Power Electronics*, vol. 31, no. 1, pp. 135-151, 2015.
- [3] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation control and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron*, vol. 30, no. 1, pp. 37-53, 2015.
- [4] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular Cascaded H-Bridge Multilevel PV Inverter With Distributed MPPT for Grid-Connected Applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1722-1731, 2015, doi: 10.1109/TIA.2014.2354396.
- [5] A. K. Sadigh, M. Abarzadeh, K. A. Corzine, and V. Dargahi, "A New Breed of Optimized Symmetrical and Asymmetrical Cascaded Multilevel Power Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 4, pp. 1160-1170, 2015, doi: 10.1109/JESTPE.2015.2459011.
- [6] B. Ahmed, K. A. Aganah, M. Ndoeye, M. A. Arif, C. Luciano, and G. V. Murphy, "Single-phase cascaded multilevel inverter topology for distributed DC sources," in *2017 IEEE 8th Annual Ubiquitous Computing, Electronics and Mobile Communication Conference (UEMCON)*, 19-21 Oct. 2017 2017, pp. 514-519, doi: 10.1109/UEMCON.2017.8248980.
- [7] D. Karwatzki and A. Mertens, "Generalized Control Approach for a Class of Modular Multilevel Converter Topologies," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 2888-2900, 2018, doi: 10.1109/TPEL.2017.2703917.
- [8] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Transactions on industrial electronics*, vol. 51, no. 3, pp. 641-660, 2004.
- [9] V. M. Lopez-Martin, F. J. Azcondo, and A. Pigazo, "Power quality enhancement in residential smart grids through power factor correction stages," *IEEE Transactions on industrial electronics*, vol. 65, no. 11, pp. 8553-8564, 2018.
- [10] M. Bollen, J. Zhong, F. Zavoda, J. Meyer, A. McEachern, and F. C. Lopez, "Power quality aspects of smart grids," in *EPRI PQ and Smart Distribution. Conference and Exhibition: 14/06/2010-17/06/2010*, 2010.
- [11] O. Ceaki, G. Seritan, R. Vatu, and M. Mancasi, "Analysis of power quality improvement in smart grids," in *2017 10th International Symposium on Advanced Topics in Electrical Engineering (ATEE)*, 2017: IEEE, pp. 797-801.

- [12] B. Singh, S. Gairola, B. N. Singh, A. Chandra, and K. Al-Haddad, "Multipulse AC–DC converters for improving power quality: A review," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 260-281, 2008.
- [13] F. Nejabatkhah, Y. W. Li, and H. Tian, "Power quality control of smart hybrid AC/DC microgrids: An overview," *IEEE Access*, vol. 7, pp. 52295-52318, 2019.
- [14] L. Yao, B. Yang, H. Cui, J. Zhuang, J. Ye, and J. Xue, "Challenges and progresses of energy storage technology and its application in power systems," *Journal of Modern Power Systems and Clean Energy*, vol. 4, no. 4, pp. 519-528, 2016.
- [15] M. Faisal, M. A. Hannan, P. J. Ker, A. Hussain, M. B. Mansor, and F. Blaabjerg, "Review of energy storage system technologies in microgrid applications: Issues and challenges," *Ieee Access*, vol. 6, pp. 35143-35164, 2018.
- [16] V. A. Boicea, "Energy storage technologies: The past and the present," *Proceedings of the IEEE*, vol. 102, no. 11, pp. 1777-1794, 2014.
- [17] M. S. Whittingham, "History, evolution, and future status of energy storage," *Proceedings of the IEEE*, vol. 100, no. Special Centennial Issue, pp. 1518-1534, 2012.
- [18] J. Araiza, J. Hambrick, J. Moon, M. Starke, and C. Vartanian, "Grid Energy-Storage Projects: Engineers Building and Using Knowledge in Emerging Projects," *IEEE Electrification Magazine*, vol. 6, no. 3, pp. 14-19, 2018.
- [19] R. Baxter, I. Gyuk, R. H. Byrne, and B. R. Chalamala, "Engineering Energy-Storage Projects: Applications and Financial Aspects," *IEEE Electrification Magazine*, vol. 6, no. 3, pp. 4-12, 2018.
- [20] S. K. Mazumder, "Energy Storage: A Power Electronics System View," *IEEE Power Electronics Magazine*, vol. 6, no. 4, pp. 36-38, 2019.
- [21] M. G. Molina, "Energy storage and power electronics technologies: A strong combination to empower the transformation to the smart grid," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2191-2219, 2017.
- [22] S. Hester, "IEEE 929–2000 Recommended Practice for Utility Interface of Photovoltaic(PV) Systems," in *Workshop Proceedings-Solar Electric Power Association*, 2002.
- [23] J. Wiles, "Photovoltaic power systems and the 2005 National Electrical Code: suggested practices," *Sandia National Laboratories*, 2005.
- [24] U. Std, "1741. Inverters, converters, and controllers for use in independent power systems," ed: IEEE, 2002.
- [25] S. Sajadian and E. C. d. Santos, "Three-phase DC-AC converter with five-level four-switch characteristic," in *2014 Power and Energy Conference at Illinois (PECI)*, 28 Feb.-1 March 2014 2014, pp. 1-6, doi: 10.1109/PECI.2014.6804556.
- [26] J. Korhonen, A. Sankala, J. Ström, P. Silventoinen, and A. Doktor, "Five-level inverter with a neutral point connection and a flying capacitor," in *2014 16th European Conference on Power Electronics and Applications*, 26-28 Aug. 2014 2014, pp. 1-7, doi: 10.1109/EPE.2014.6910934.
- [27] X. Yuan, "A new five-level converter for low-voltage motor drive applications," in *2014 17th International Conference on Electrical Machines and Systems (ICEMS)*, 22-25 Oct. 2014 2014, pp. 2969-2974, doi: 10.1109/ICEMS.2014.7014005.

- [28] A. Masaoud, H. W. Ping, S. Mekhilef, and A. Taallah, "Novel configuration for multilevel DC-link three-phase five-level inverter," *IET Power Electronics*, vol. 7, no. 12, pp. 3052-3061, 2014, doi: 10.1049/iet-pel.2013.0812.
- [29] H. Vahedi, P. Labbé, and K. Al-Haddad, "Sensor-Less Five-Level Packed U-Cell (PUC5) Inverter Operating in Stand-Alone and Grid-Connected Modes," *IEEE Transactions on Industrial Informatics*, vol. 12, no. 1, pp. 361-370, 2016, doi: 10.1109/TII.2015.2491260.
- [30] M. Saeedian, S. M. Hosseini, and J. Adabi, "A Five-Level Step-Up Module for Multilevel Inverters: Topology, Modulation Strategy, and Implementation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 4, pp. 2215-2226, 2018, doi: 10.1109/JESTPE.2018.2819498.
- [31] A. M. R and K. Sivakumar, "A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7569-7577, 2015, doi: 10.1109/TIE.2015.2455523.
- [32] L. He and C. Cheng, "A Flying-Capacitor-Clamped Five-Level Inverter Based on Bridge Modular Switched-Capacitor Topology," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7814-7822, 2016, doi: 10.1109/TIE.2016.2607155.
- [33] S. P. Gautam, L. Kumar, S. Gupta, and N. Agrawal, "A Single-Phase Five-Level Inverter Topology With Switch Fault-Tolerance Capabilities," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2004-2014, 2017, doi: 10.1109/TIE.2016.2626368.
- [34] M. Narimani, B. Wu, and N. R. Zargari, "A Novel Five-Level Voltage Source Inverter With Sinusoidal Pulse Width Modulator for Medium-Voltage Applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1959-1967, 2016, doi: 10.1109/TPEL.2015.2440656.
- [35] M. Aly, E. M. Ahmed, and M. Shoyama, "A New Single-Phase Five-Level Inverter Topology for Single and Multiple Switches Fault Tolerance," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9198-9208, 2018, doi: 10.1109/TPEL.2018.2792146.
- [36] R. Naderi, A. K. Sadigh, and K. M. Smedley, "Dual flying capacitor active-neutral-point-clamped multilevel converter," *IEEE transactions on power electronics*, vol. 31, no. 9, pp. 6476-6484, 2015.
- [37] V. Monteiro, J. C. Ferreira, A. A. N. Meléndez, and J. L. Afonso, "Model predictive control applied to an improved five-level bidirectional converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 9, pp. 5879-5890, 2016.
- [38] R. S. Leite, J. L. Afonso, and V. Monteiro, "A novel multilevel bidirectional topology for on-board EV battery chargers in smart grids," *Energies*, vol. 11, no. 12, p. 3453, 2018.
- [39] J. Xu, J. Li, J. Zhang, L. Shi, X. Jia, and C. Zhao, "Open-loop voltage balancing algorithm for two-port full-bridge MMC-HVDC system," *International Journal of Electrical Power & Energy Systems*, vol. 109, pp. 259-268, 2019/07/01/ 2019, doi: <https://doi.org/10.1016/j.ijepes.2019.01.032>.
- [40] J. Wang, X. Han, H. Ma, and Z. Bai, "Analysis and Injection Control of Circulating Current for Modular Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2280-2290, 2019, doi: 10.1109/TIE.2018.2808901.
- [41] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE*

- Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1631-1656, 2017, doi: 10.1109/JESTPE.2017.2742938.
- [42] D. Zhou, S. Yang, and Y. Tang, "Model-predictive current control of modular multilevel converters with phase-shifted pulsewidth modulation," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 6, pp. 4368-4378, 2018.
- [43] J. Hu, M. Xiang, L. Lin, M. Lu, J. Zhu, and Z. He, "Improved Design and Control of FBSM MMC With Boosted AC Voltage and Reduced DC Capacitance," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 1919-1930, 2018, doi: 10.1109/TIE.2017.2739679.
- [44] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular Multilevel Converter With Series and Parallel Module Connectivity: Topology and Control," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 203-215, 2015, doi: 10.1109/TPEL.2014.2310225.
- [45] J. Xu, M. Feng, H. Liu, S. Li, X. Xiong, and C. Zhao, "The diode-clamped half-bridge MMC structure with internal spontaneous capacitor voltage parallel-balancing behaviors," *International Journal of Electrical Power & Energy Systems*, vol. 100, pp. 139-151, 2018.
- [46] P. Hu and D. Jiang, "A level-increased nearest level modulation method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1836-1842, 2014.
- [47] Z. Li, R. L. F. S. Sha, Z. Yu, A. V. Peterchev, and S. M. Goetz, "Module Implementation and Modulation Strategy for Sensorless Balancing in Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8405-8416, 2019, doi: 10.1109/TPEL.2018.2886147.
- [48] Y. Jin *et al.*, "A Novel Submodule Voltage Balancing Scheme for Modular Multilevel Cascade Converter—Double-Star Chopper-Cells (MMCC-DSCC) based STATCOM," *IEEE Access*, 2019.
- [49] S. M. Goetz, Z. Li, X. Liang, C. Zhang, S. M. Lukic, and A. V. Peterchev, "Control of modular multilevel converter with parallel connectivity—Application to battery systems," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8381-8392, 2016.
- [50] Y. Zhu, W. Zhang, J. Cheng, and Y. Li, "A novel design of reconfigurable multicell for large-scale battery packs," in *2018 International Conference on Power System Technology (POWERCON)*, 6-8 Nov. 2018 2018, pp. 1445-1452, doi: 10.1109/POWERCON.2018.8602284.
- [51] Z. Li, R. Lizana, A. V. Peterchev, and S. M. Goetz, "Distributed balancing control for modular multilevel series/parallel converter with capability of sensorless operation," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 1-5 Oct. 2017 2017, pp. 1787-1793, doi: 10.1109/ECCE.2017.8096011.
- [52] J. Rodriguez, L. Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, 2002, doi: 10.1109/TIE.2002.801052.
- [53] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930-2945, 2007, doi: 10.1109/TIE.2007.907044.

- [54] S. Kouro *et al.*, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553-2580, 2010, doi: 10.1109/TIE.2010.2049719.
- [55] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A Survey on Cascaded Multilevel Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197-2206, 2010, doi: 10.1109/TIE.2009.2030767.
- [56] Y. Li, Y. Wang, and B. Q. Li, "Generalized theory of phase-shifted carrier PWM for cascaded H-bridge converters and modular multilevel converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 589-605, 2015.
- [57] B. Ge and P. Fang Zheng, "An effective control technique for medium-voltage high power induction motor drives," in *2008 34th Annual Conference of IEEE Industrial Electronics*, 10-13 Nov. 2008 2008, pp. 3195-3200, doi: 10.1109/IECON.2008.4758472.
- [58] R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, and K. Gopakumar, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," *IEE Proceedings - Electric Power Applications*, vol. 152, no. 2, pp. 297-309, 2005, doi: 10.1049/ip-epa:20045047.
- [59] B. Vinod, M. Baiju, and G. Shiny, "Five-level inverter-fed space vector based direct torque control of open-end winding induction motor drive," *IEEE Transactions on Energy Conversion*, vol. 33, no. 3, pp. 1392-1401, 2018.
- [60] I. Ahmed, V. B. Borghate, A. Matsa, P. M. Meshram, H. M. Suryawanshi, and M. A. Chaudhari, "Simplified Space Vector Modulation Techniques for Multilevel Inverters," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8483-8499, 2016, doi: 10.1109/TPEL.2016.2520078.
- [61] K. Dae-Wook, L. Yo-Han, S. Bum-Seok, C. Chang-Ho, and H. Dong-Seok, "An improved carrier-based SVPWM method using leg voltage redundancies in generalized cascaded multilevel inverter topology," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 180-187, 2003, doi: 10.1109/TPEL.2002.807187.
- [62] W. Li, J. Hu, S. Hu, H. Yang, H. Yang, and X. He, "Capacitor voltage balance control of five-level modular composited converter with hybrid space vector modulation," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5629-5640, 2017.
- [63] J. MA and P. Anitha, "Mitigation of Voltage Imbalance in the DC link of a Split Link Four Wire Inverter."
- [64] G. Graditi, G. Adinolfi, N. Femia, and M. Vitelli, "Comparative analysis of synchronous rectification boost and diode rectification boost converter for DMPPT applications," in *2011 IEEE International Symposium on Industrial Electronics*, 2011: IEEE, pp. 1000-1005.
- [65] F. H. Reynolds, "Thermally accelerated aging of semiconductor components," *Proceedings of the IEEE*, vol. 62, no. 2, pp. 212-222, 1974.
- [66] Y. Kyono, "Switching-mode power supply having a synchronous rectifier," ed: Google Patents, 2006.
- [67] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6319-6331, 2014.

